IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Yi Ding		
Assignee:	Mosel Vitelic, Inc.		
Title:	Nonvolatile Memory Fabrication Methods Comprising Lateral Recessing of Dielectric Sidewalls at Substrate Isolation Regions		
Application No.:	10/678,317	Filing Date:	October 3, 2003
Examiner:	Unknown	Group Art Unit:	Unassigned
Docket No.:	M-15210 US		

San Jose, California
December 18, 2003

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR § 1.97(b)

Dear Sir:

Pursuant to 37 CFR § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed except for the United States Patents and United States. The relevance of the Japanese language document is explained in the enclosed document from Patent Abstracts of Japan.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;

2. a representation that a search has been made, other than as described above; or

3. an admission that the information cited herein is, or is considered to be material to patentability as defined in § 1.56(b).

No fee is believed to be required. If a fee is required for this Information Disclosure Statement, please charge the fee to Deposit Account No. 50-2257. This paper is being submitted in duplicate.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 18, 2003.

Michael Shenker 12-18-03

Attorney for Applicant(s) Date of Signature

Respectfully submitted,

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U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Serial No.
	M-15210 US	10/678,317
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Yi Ding	
	Filing Date	Group
	October 3, 2003	Unassigned

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,222,225	24 Apr. 2001	Nakamura et al.			
	AB	6,228,713	8 May 2001	Pradeep et al.			
	AC	6,323,085	27 Nov. 2001	Sandhu et al.			
	AD	5,940,717	17 Aug. 1999	Rengarajan et al.			
	AE	6,127,215	3 Oct 2000	Joachim et al.			
	AF	6,130,129	10 Oct. 2000	Chen			
	AG	6,200,856	13 Mar. 2001	Chem			
	AH	6,319,794	20 Nov. 2001	Akatsu et al.			
	AI	6,355,524	12 Mar. 2002	Tuan et al.			
	AJ	6,518,618	11 Feb. 2003	Fazio et al.			

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AK	2000-174242	23 Jun. 2000	JP				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AL	Aritome, S. et al., "A 0.67um^2 Self-Aligned Shallow Trench Isolation Cell (SA-STI Cell) For 3V-only 256Mbit NAND EEPROMs," International Electron Devices meeting 1994, San Francisco, CA, December 11-14, 1994, pages 94-61 – 94-64.
	AM	Keeney, Stephen N., "A 130nm Generation High Density Etox™ Flash Memory Technology, Intel, Corporation, Santa Clara, California, USA, 42 sheets.
	AN	United States Patent Application No. 10/266,378 entitled "Floating Gate Memory Structures And Fabrication Methods," filed on October 7, 2002, Inventor: Chia-Shun Hsiao, Attorney Docket No. M-12200 US.
	AO	United States Patent Application No. 10/262,785, entitled "Floating Gate Memory Fabrication Methods Comprising A Field Dielectric Etch With A Horizontal Etch Component," filed on October 1, 2002, Inventor: Yi Ding, Attorney Docket No.: M-12841 US.
	AP	Silicon, Flash and Other Non-Volatile Memory Technologies, http://www.intel.com/research/silicon/flash.htm, September 12, 2002, pages 1-4.
	AQ	Patent Abstracts of Japan of JP 2000-174242.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.